

See

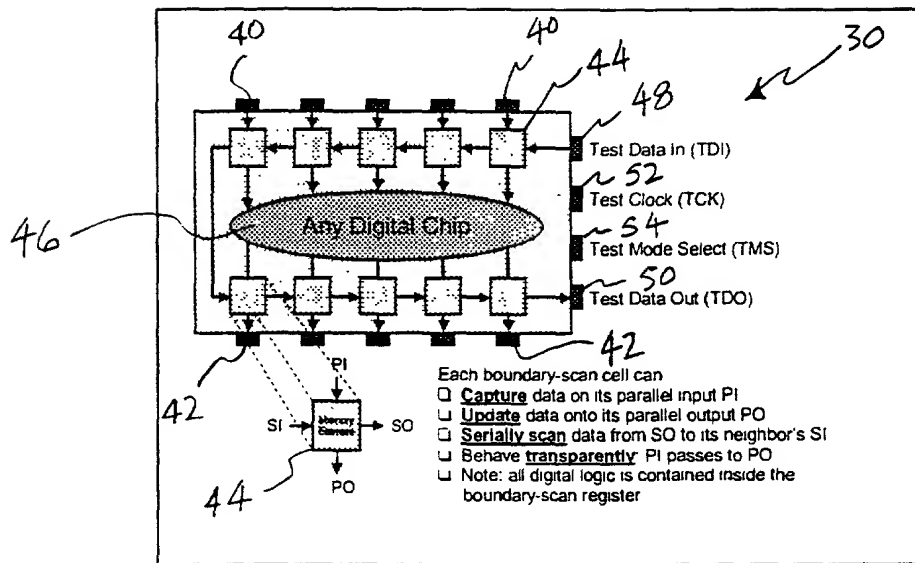


Figure 2: Principle of Boundary-Scan Architecture  
1 (PRIOR ART)

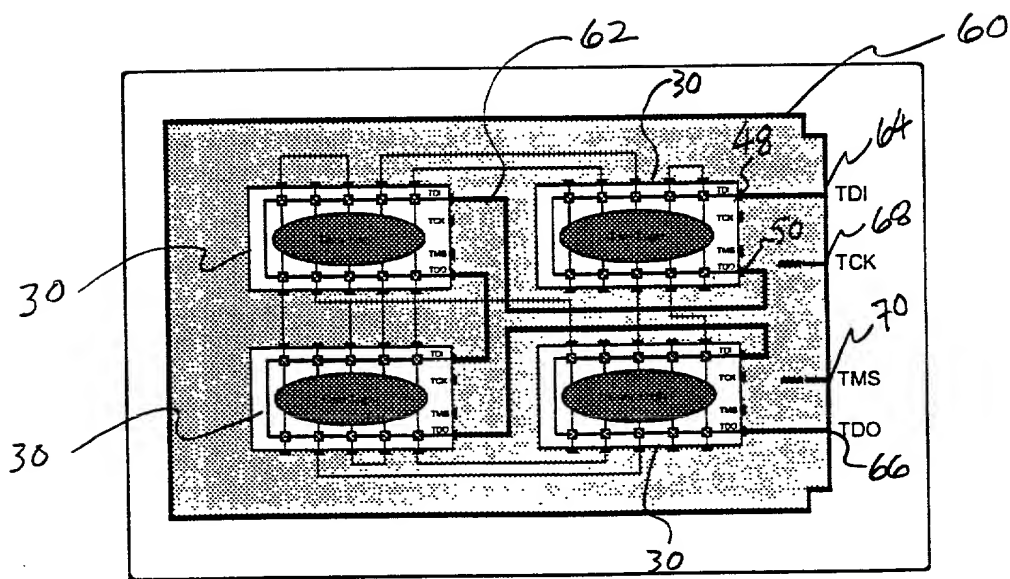


Figure 1: Using the Boundary-Scan Path  
 2 (PRIOR ART)

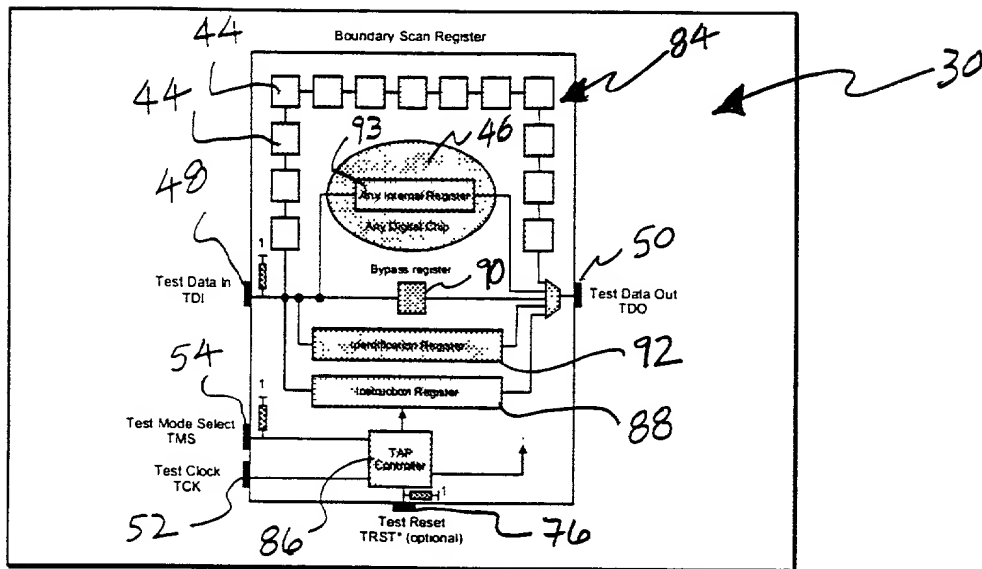


Figure 8: ~~IEEE 1149.1 Chip Architecture~~  
(Prior Art)

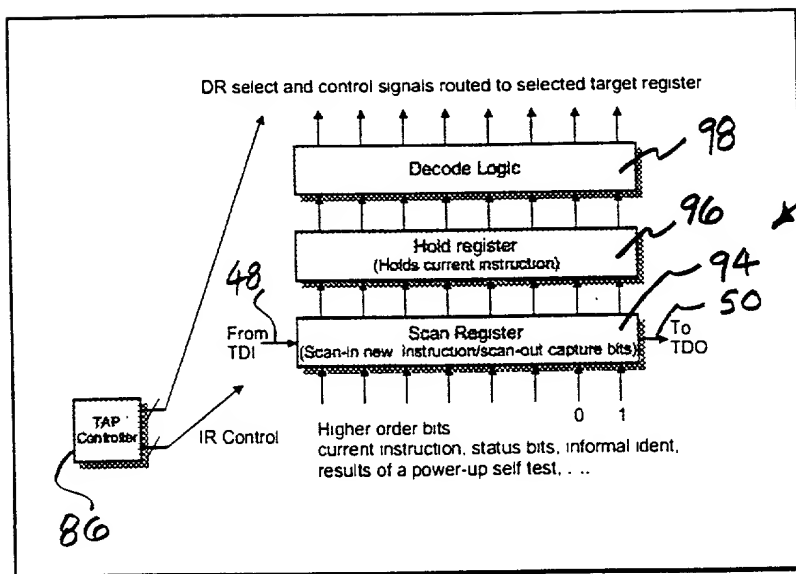


Figure 8: The Instruction Register  
4 (PRIORITY)

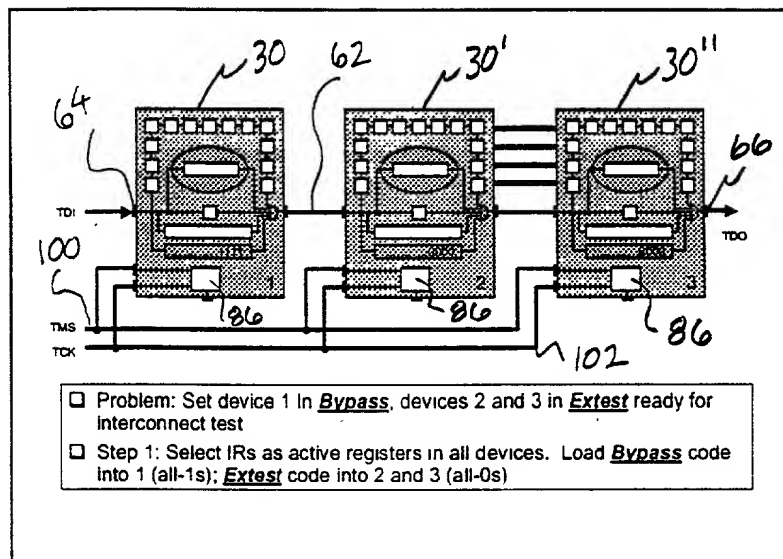


Figure 10: Using the Instruction Register — Step 1  
5 (PRIOR ART)

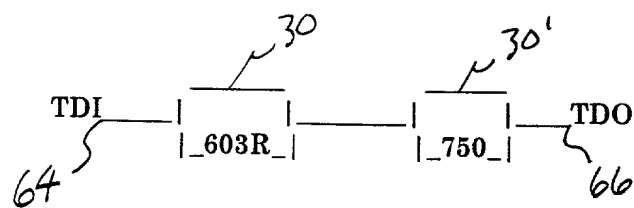


Fig. 16

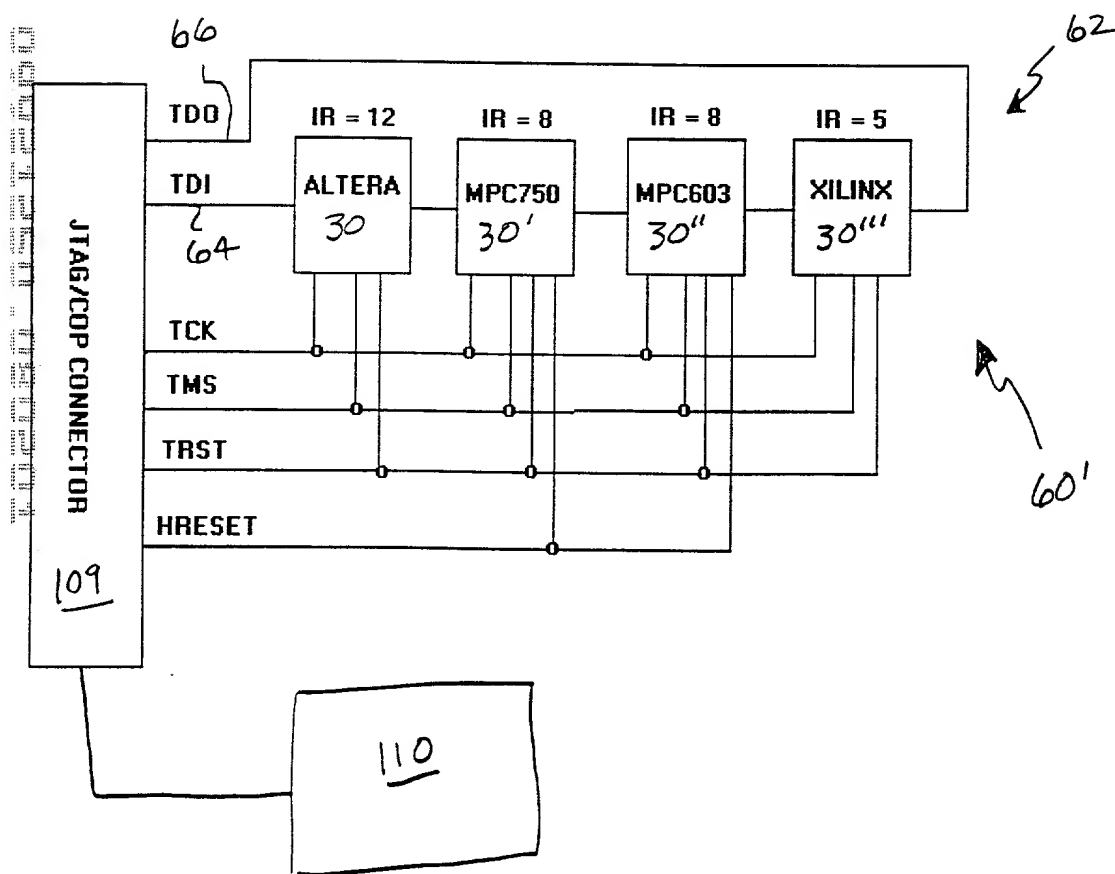


Fig. 27A

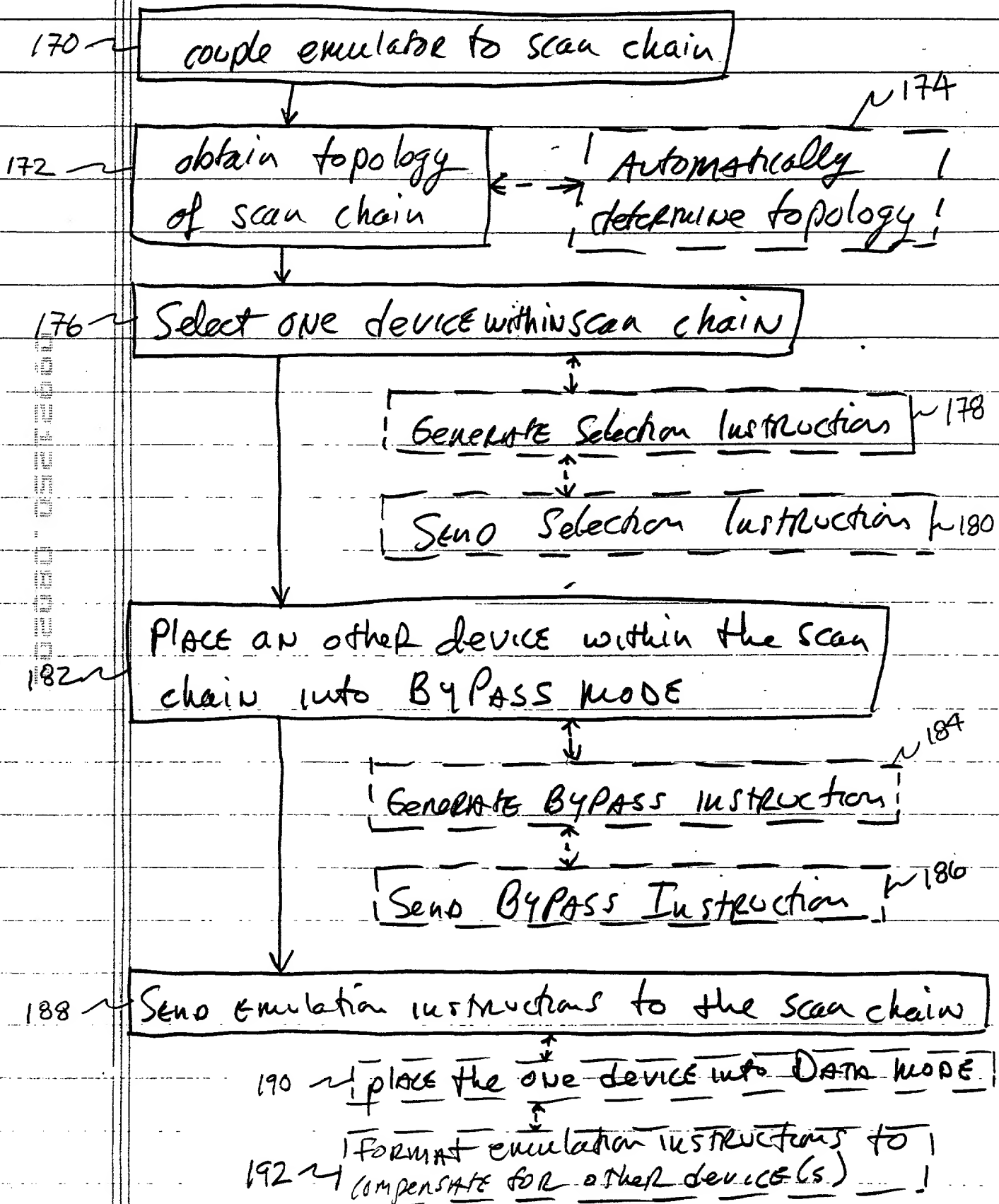


Fig. 7B

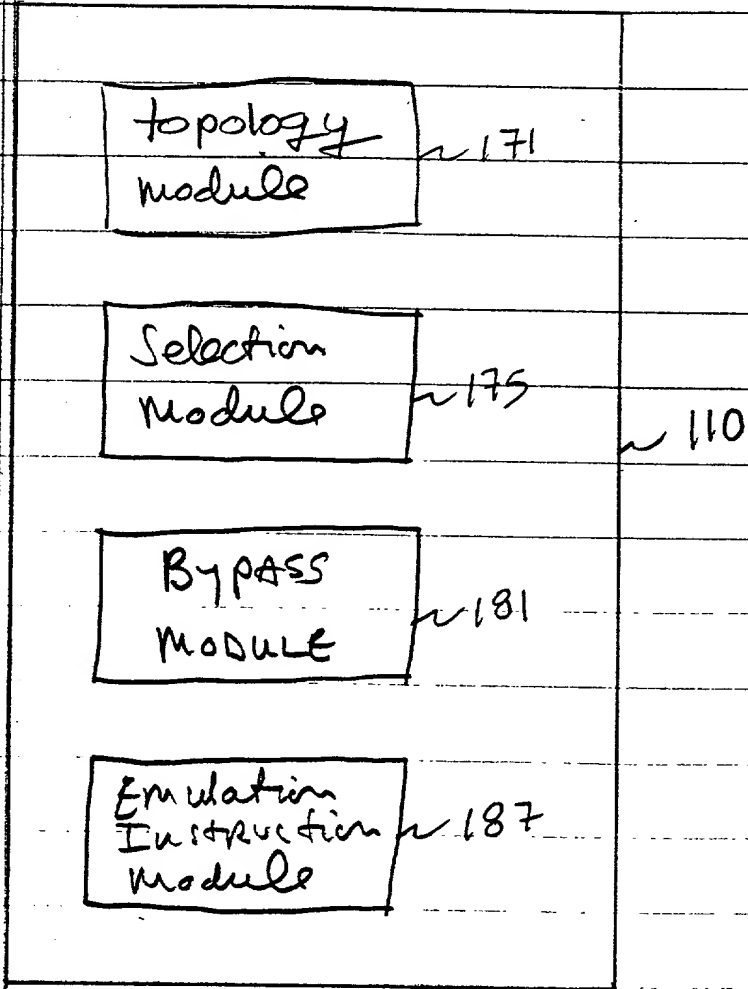


Fig. 7C



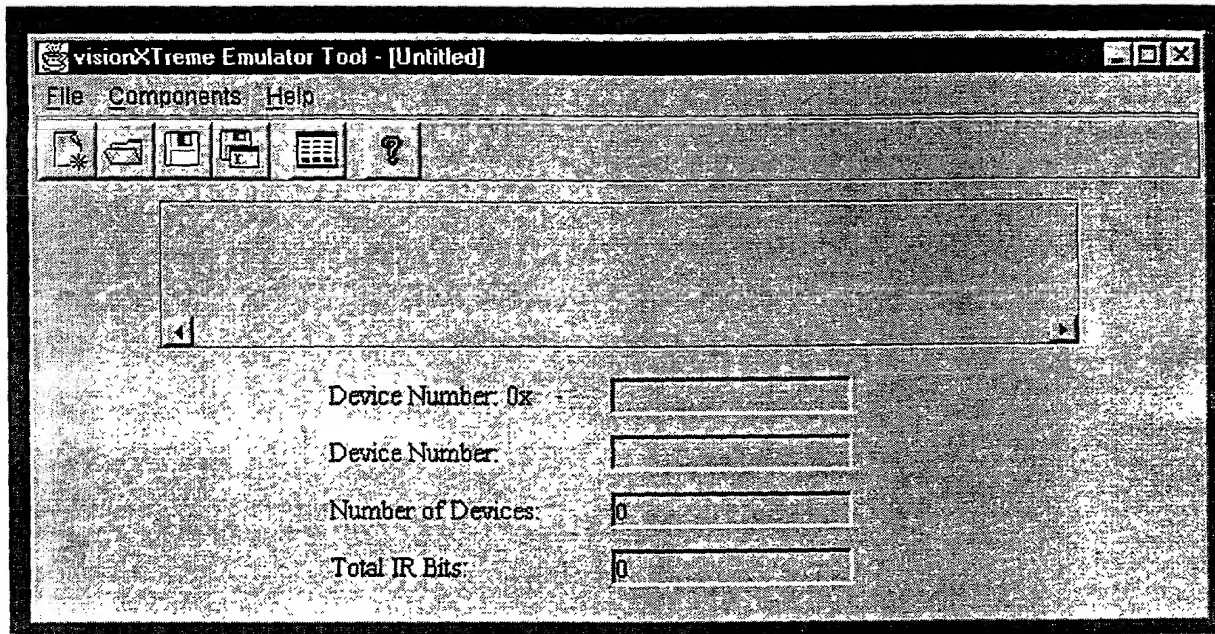


Fig. 8

200

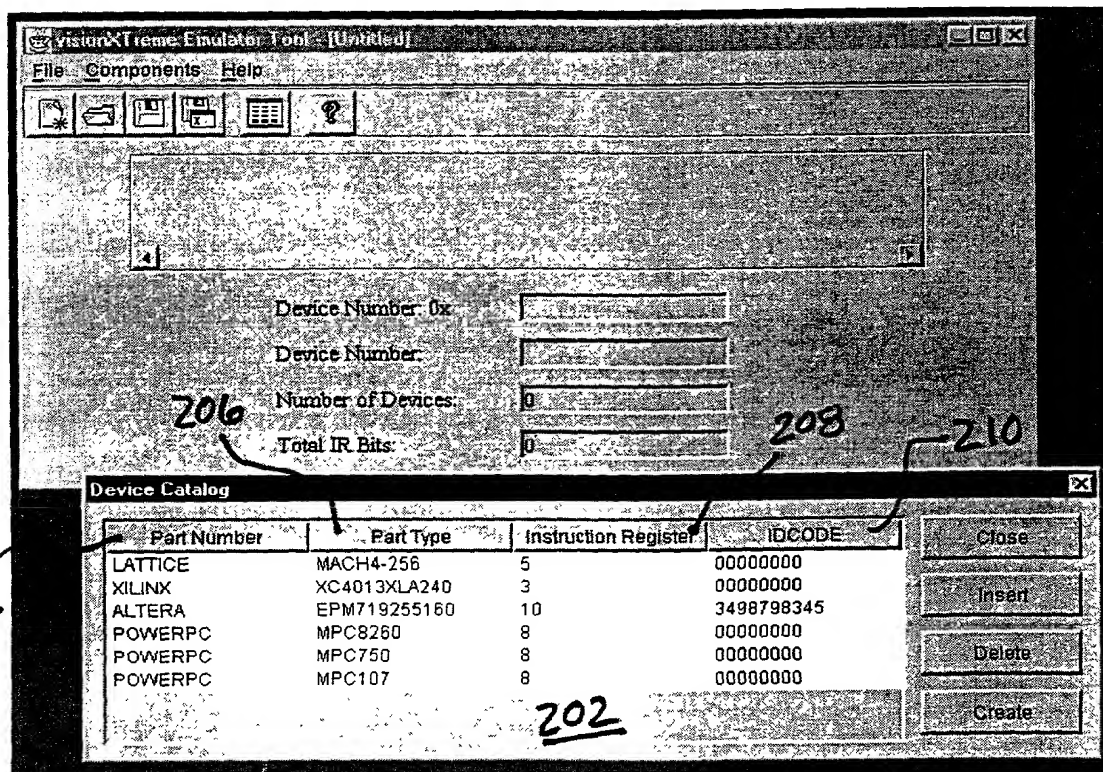


Fig. 9

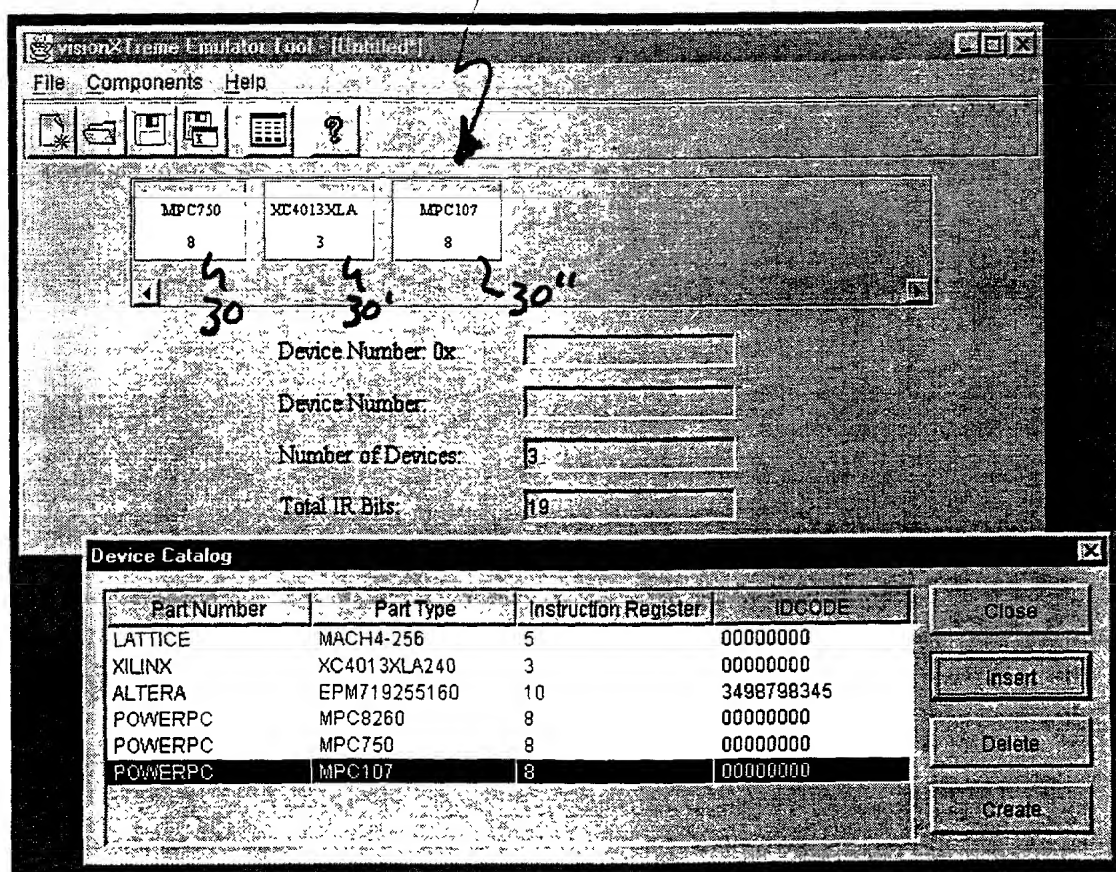


Fig. 10

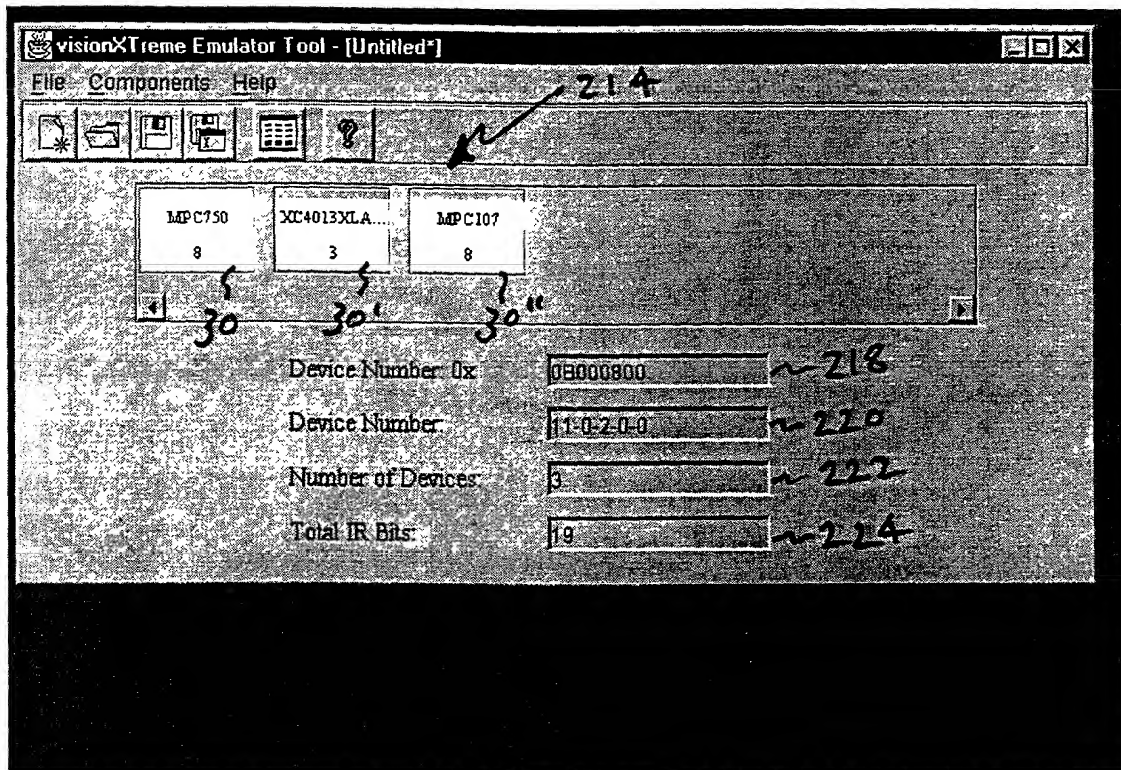


Fig. 811

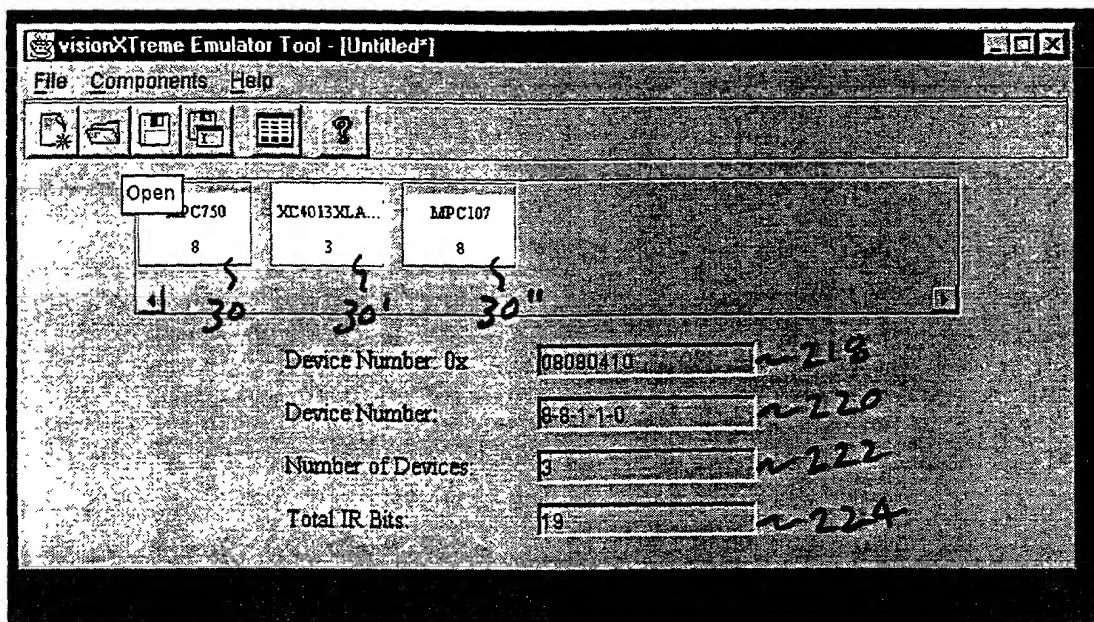


Fig. 812